IN THE CLAIMS

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1. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a data gate circuit that transmits a data gate signal;

a data circuit that transmits or receives data under ~~the~~ control of the data gate signal;

a media gate circuit that transmits a media gate signal;

a mode selection circuit that transmits mode selection information under ~~the~~ control of the media gate signal; and

a buffer attention circuit that receives a buffer attention signal.

2. (Original) The latency-independent interface of claim 1, wherein the mode selection information comprises tag information and control information.

3. (Original) The latency-independent interface of claim 2, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

4. (Original) The latency-independent interface of claim 3, wherein the control information further comprises a reset command.

5. (Original) The latency-independent interface of claim 3, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

6. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a data gate circuit that receives a data gate signal;

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a data circuit that transmits or receives data under ~~the~~ control of the data gate signal;

a media gate circuit that receives a media gate signal;

a mode selection circuit that receives mode selection information under ~~the~~ control of the media gate signal; and

a buffer attention circuit that transmits a buffer attention signal.

7. (Original) The latency-independent interface of claim 6, wherein the mode selection information comprises tag information and control information.

8. (Original) The latency-independent interface of claim 7, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

9. (Original) The latency-independent interface of claim 8, wherein the control information further comprises a reset command.

10. (Original) The latency-independent interface of claim 8, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

11. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

a first data gate circuit that transmits a data gate signal;

a first data circuit that transmits or receives data under ~~the~~ control of the data gate signal;

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a first media gate circuit that transmits a media gate signal;

a first mode selection circuit that transmits mode selection information under ~~the~~ control of the media gate signal;

a first buffer attention circuit that receives a buffer attention signal;

a second data gate circuit that receives the data gate signal;

a second data circuit that transmits or receives data under the control of ~~the~~ data gate signal;

a second media gate circuit that receives the media gate signal;

a second mode selection circuit that receives mode selection information under ~~the~~ control of the media gate signal; and

a second buffer attention circuit that transmits ~~a~~ the buffer attention signal.

12. (Original) The latency-independent interface of claim 11, wherein the mode selection information comprises tag information and control information.

13. (Original) The latency-independent interface of claim 12, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

14. (Original) The latency-independent interface of claim 13, wherein the control information further comprises a reset command.

15. (Original) The latency-independent interface of claim 13, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

16. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for transmitting a data gate signal;

data circuit means for transmitting or receiving data under ~~the~~ control of the data gate signal;

media gate circuit means for transmitting a media gate signal;

mode selection circuit means for transmitting mode selection information under ~~the~~ control of the media gate signal; and

buffer attention circuit means for receiving a buffer attention signal.

17. (Original) The latency-independent interface of claim 16, wherein the mode selection information comprises tag information and control information.

18. (Original) The latency-independent interface of claim 17, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

19. (Original) The latency-independent interface of claim 18, wherein the control information further comprises a reset command.

20. (Original) The latency-independent interface of claim 18, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

21. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

data gate circuit means for receiving a data gate signal;

data circuit means for transmitting or receiving data under ~~the~~ control of the data gate signal;

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media gate circuit means for receiving a media gate signal;

mode selection circuit means for receiving mode selection information under ~~the~~ control of the media gate signal; and

buffer attention circuit means for transmitting a buffer attention signal.

22. (Original) The latency-independent interface of claim 21, wherein the mode selection information comprises tag information and control information.

23. (Original) The latency-independent interface of claim 22, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

24. (Original) The latency-independent interface of claim 23, wherein the control information further comprises a reset command.

25. (Original) The latency-independent interface of claim 23, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

26. (Currently Amended) A latency-independent interface between first and second hardware components, comprising:

first data gate circuit means for transmitting a data gate signal;

first data circuit means for transmitting or receiving data under ~~the~~ control of the data gate signal;

first media gate circuit means for transmitting a media gate signal;

first mode selection circuit means for transmitting mode selection information under ~~the~~ control of the media gate signal;

first buffer attention circuit means for receiving a buffer attention signal;

second data gate circuit means for receiving the data gate signal;

second data circuit means for transmitting or receiving data under ~~the~~ control of the data gate signal;

second media gate circuit means for receiving the media gate signal;

second mode selection circuit means for receiving mode selection information under ~~the~~ control of the media gate signal; and

second buffer attention circuit means for transmitting a buffer attention signal.

27. (Original) The latency-independent interface of claim 26, wherein the mode selection information comprises tag information and control information.

28. (Original) The latency-independent interface of claim 27, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

29. (Original) The latency-independent interface of claim 28, wherein the control information further comprises a reset command.

30. (Original) The latency-independent interface of claim 28, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

31. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

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transmitting a media gate signal;

transmitting mode selection information under the control of the media gate signal; and

receiving a buffer attention signal.

32. (Original) The method of claim 31, wherein the mode selection information comprises tag information and control information.

33. (Original) The method of claim 32, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

34. (Original) The method of claim 33, wherein the control information further comprises a reset command.

35. (Original) The method of claim 33, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

36. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

receiving a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

receiving a media gate signal;

receiving mode selection information under ~~the~~ control of the media gate signal; and

transmitting a buffer attention signal.

37. (Original) The method of claim 36, wherein the mode selection information comprises tag information and control information.

38. (Original) The method of claim 37, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

39. (Original) The method of claim 38, wherein the control information further comprises a reset command.

40. (Original) The method of claim 38, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

41. (Currently Amended) A method of transmitting and receiving signals between first and second hardware components, comprising the steps of:

transmitting and receiving a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

transmitting and receiving a media gate signal;

transmitting and receiving mode selection information under ~~the~~ control of the media gate signal; and

transmitting and receiving a buffer attention signal.

42. (Original) The method of claim 41, wherein the mode selection information comprises tag information and control information.

43. (Original) The method of claim 42, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises

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commands that indicate whether associated data is continued from a previous location or from a new location.

44. (Original) The method of claim 43, wherein the control information further comprises a reset command.

45. (Original) The method of claim 43, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

46. (Currently Amended) An interface protocol between at least two hardware components, comprising:

a transmitted data gate signal;

a data signal carrying data that is transmitted or received under ~~the~~ control of the data gate signal;

a transmitted media gate signal;

a mode selection signal carrying mode selection information that is transmitted under ~~the~~ control of the media gate signal; and

a received buffer attention signal.

47. (Original) The interface protocol of claim 46, wherein the mode selection information comprises tag information and control information.

48. (Original) The interface protocol of claim 47, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

49. (Original) The interface protocol of claim 48, wherein the control information further comprises a reset command.

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50. (Original) The interface protocol of claim 48, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

51. (Currently Amended) An interface protocol between at least two hardware components, comprising:

a received data gate signal;

a data signal carrying data that is transmitted or received under ~~the~~ control of the data gate signal;

a received a media gate signal;

a mode selection signal carrying mode selection information that is received under ~~the~~ control of the media gate signal; and

a transmitted buffer attention signal.

52. (Original) The interface protocol of claim 51, wherein the mode selection information comprises tag information and control information.

53. (Original) The interface protocol of claim 52, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

54. (Original) The interface protocol of claim 53, wherein the control information further comprises a reset command.

55. (Original) The interface protocol of claim 53, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

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56. (Currently Amended) An interface protocol between at least two hardware components, comprising:

a data gate signal transmitted by a first hardware component and received by a second hardware component;

a data signal that transmits data between the first and second hardware components under ~~the~~ control of the data gate signal;

a media gate signal transmitted by the first hardware component and received by the second hardware component;

a mode selection signal that transmits mode selection information from the first hardware component to the second hardware component under ~~the~~ control of the media gate signal; and

a buffer attention signal transmitted by the second hardware component and received by the first hardware component.

57. (Original) The interface protocol of claim 56, wherein the mode selection information comprises tag information and control information.

58. (Original) The interface protocol of claim 57, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

59. (Original) The interface protocol of claim 58, wherein the control information further comprises a reset command.

60. (Original) The interface protocol of claim 58, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

61. (Currently Amended) A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising instructions for:

transmitting a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

transmitting a media gate signal;

transmitting mode selection information under ~~the~~ control of the media gate signal; and

receiving a buffer attention signal.

62. (Original) The device-readable medium of claim 61, wherein the mode selection information comprises tag information and control information.

63. (Original) The device-readable medium of claim 62, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

64. (Original) The device-readable medium of claim 63, wherein the control information further comprises a reset command.

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65. (Original) The device-readable medium of claim 63, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

66. (Currently Amended) A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising instructions for:

receiving a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

receiving a media gate signal;

receiving mode selection information under ~~the~~ control of the media gate signal; and

transmitting a buffer attention signal.

67. (Original) The device-readable medium of claim 66, wherein the mode selection information comprises tag information and control information.

68. (Original) The device-readable of claim 67, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

69. (Original) The device-readable medium of claim 68, wherein the control information further comprises a reset command.

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70. (Original) The device-readable medium of claim 68, wherein the control information further comprises size information comprising a size command that indicates size of associated data.

71. (Currently Amended) A device-readable medium embodying a program of instructions for execution by a device for performing a method of transmitting and receiving signals between first and second hardware components, the program of instructions comprising instructions for:

transmitting and receiving a data gate signal;

transmitting or receiving data under ~~the~~ control of the data gate signal;

transmitting and receiving a media gate signal;

transmitting and receiving mode selection information under ~~the~~ control of the media gate signal; and

transmitting and receiving a buffer attention signal.

72. (Original) The device-readable medium of claim 71, wherein the mode selection information comprises tag information and control information.

73. The device-readable medium of claim 72, wherein the tag information comprises a tag command that identifies a location of associated data, and the control information comprises commands that indicate whether associated data is continued from a previous location or from a new location.

74. (Original) The device-readable medium of claim 73, wherein the control information further comprises a reset command.

75. (Original) The device-readable medium of claim 73, wherein the control information further comprises size information comprising a size command that indicates size of associated data.